IN THE CLAIMS:

Please amend claims 3 - 6, as shown in the complete list of claims that is presented below.

1. (previously presented) An ONO flash memory array for reducing disturbance between adjacent memory cells, comprising:

a substrate having ~~a~~ first and second buried diffusion regions;

a channel between the first and second buried diffusion regions;

an ONO layer above the channel for memory storage;

a first pocket of a first concentration implanted on one side of the channel close to the first buried diffusion region; and

a second pocket of a second concentration implanted on the other side of the channel close to the second buried diffusion region, wherein the first concentration is higher than the second concentration.

Claim 2 (cancelled).

3. (currently amended) An ONO flash memory array for reducing disturbance between first and second adjacent memory cells, comprising:

a substrate having ~~a~~ first and second buried diffusion regions, the second buried diffusion region having a first portion in the first memory cell and a second portion in the second memory cell;

a channel in the first memory between the first buried diffusion region and the first portion of the second buried diffusion ~~region.~~ region;

an ONO layer above the channel for memory storage in the first memory cell;

a first implanted pocket at the first portion of the second buried diffusion~~.~~ region, the first pocket having a first concentration; and

a second implanted pocket at the second portion of the second diffusion region, the second pocket having a second concentration that is different from the first concentration.

4. (currently amended) An ONO flash memory array for reducing disturbance between first and second adjacent memory cells, comprising:

a substrate having first source/drain and second ~~buried diffusion~~ source/drain regions, the second ~~buried diffusion~~ source/drain region having a first portion in the first memory cell and a second portion in the second memory cell;

a channel in the first memory cell between the first ~~buried diffusion~~ source/drain region and the first portion of the second ~~buried diffusion~~ source/drain region;

an ONO layer above the channel for memory storage in the first memory cell; and

~~means for providing the second buried diffusion region with~~ an implanted pocket arrangement nearby the second source/drain region that is asymmetrical with respect to the first and second portions thereof.

5. (currently amended) The memory array of claim 4, wherein the ~~means~~ implanted pocket arrangement comprises an implanted pocket at one of the portions of the second ~~buried diffusion~~ source/drain region, the other portion lacking a pocket.

6. (currently amended) The memory array of claim 4, wherein the ~~means~~ implanted pocket arrangement comprises a first implanted pocket at the first portion of the second ~~buried diffusion~~ source/drain region and a second implanted pocket at the second portion, the first and second implanted pockets having different concentrations.